

Please amend the claims as follows:

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1 1. (Twice amended) A method for developing a fully functional transparent memory module [modules
2 using] comprising an assembly of selected independent primary and backup memory parts,
3 the method comprising the steps of:
4 testing a plurality of independent memory [the] parts for failed I/O data line segments;
5 sorting the parts according to the results of the testing;
6 identifying failed and working I/O data line segments in [selected] the sorted parts;
7 selecting at least one primary part having at least one I/O data line failure, and at least one different
8 partially defective backup memory part from said sorted parts; and
9 combining [the] working I/O data line segments of different selected memory parts, including at
10 least one working I/O data line segment of at least one partially defective backup memory part and
11 working I/O data line segments of a primary part to form a fully functional transparent memory module.

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1 8. (Twice amended) A method for developing effective chip-on-board memory modules [using]
2 comprising an assembly of a selected combination of independent partially defective memory chips
3 [parts and good memory parts],
4 comprising the steps of:
5 assembling the selected chips [parts] as primary chips [parts] and backup chips [parts] onto a chip-
6 on-board memory module assembly;
7 testing the assembled module for failed I/O data lines in the chips [parts];
8 identifying [the] operating I/O data line segments in the chips [parts, including operating segments
9 in at least one of the partially defective memory parts]; and
10 combining [the] identified working I/O data line segments of a partially defective primary chip [part]
11 with a required number of working I/O data line segments of backup memory chips [parts to form an
12 effective fully functional transparent memory module].

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1 12. (Twice amended) A ^{method} ~~process~~ for patching selected partially defective independent primary memory
2 parts with selected different partially defective independent backup memory parts to form a memory
3 module functionally transparent to the user, comprising the steps of:
4 testing the primary memory parts and the backup memory parts before mounting the parts on a
5 board to;
6 identify operating and failed I/O data line segments of the primary parts and of the backup memory
7 parts;
8 determining which operating I/O data lines from the backup memory parts to use for selectively
9 patching [the] failed I/O data lines segments of the primary memory parts; and
10 substituting said determined operating I/O data lines from the backup parts for failed I/O data lines
11 in [the failed segments of] one or more primary parts to form a completed memory module.

Claim 33, line 8, after "parts" and before ";" delete "parts".

c 50. (Twice amended) ^{method} A ~~process~~ for selecting and assembling primary parts and backup parts on a chip-on-board module assembly comprising patterns of solder dot locations for the primary and backup parts, the process comprising the steps of:

- 4 performing a wafer test on a memory die;
- 5 selecting, as primary parts, partially defective dies that have a reasonable probability of being
- 6 patched successfully;
- 7 selecting, as backup parts, other partially defective dies that test to be suitable for patching [for
- 8 assembly on a PC module];
- 9 assembling the selected primary and backup parts on the PC module;
- 10 applying a plastic over coating to the assembled parts; and
- 11 [test] testing the module using a chip test applied at the module pins; and
- 12 patching failed segments of the primary parts with working segments of the backup parts.

c 51. (Twice amended) [The process of claim 50, further comprising the steps of:]

B4 ^{method} A ~~process~~ for selecting and assembling primary parts and backup parts on a chip-on-board module assembly comprising patterns of solder dot locations for the primary and backup parts, the process comprising the steps of:

- 5 performing a wafer test on a memory die;
- 6 selecting, as primary parts, dies that have a reasonable probability of being patched successfully;
- 7 selecting, as backup parts, other dies for assembly on a PC module;
- 8 assembling the selected primary and backup parts on the PC module;
- 9 applying a plastic over coating to the assembled parts; and
- 10 test the module using a chip test applied at the module ~~pins~~ ^{pins};
- 11 assigning a bar code to the module to identify failed bits;
- 12 fill in the solder-dot locations of the primary parts, the solder-dot locations of the back-up parts are
- 13 left open;
- 14 test the module on a full function circuit tester, wherein failed bits are noted, and the module is
- 15 assigned a bar-code identifying the failed bits;
- 16 generate patching instruction charts for the module, wherein the development of the patching
- 17 instruction charts includes an optimization pass designed to maximize use of smaller patch parts, leaving
- 18 the larger parts available for patching later-discovered failures;
- 19 disconnect solder-dot connections on the primary parts to isolate any failed line;
- 20 fill the solder-dot connections to patch in substitute lines, the solder-dot connections selected as
- 21 identified in the patching instruction charts;
- 22 re-test the module, including high temperature stress testing of the module.

Cancel claims 65 and 66.

1 ⁶⁵~~67~~. (Once amended) [A memory module in accordance with claim 66 wherein:] A memory module
2 comprising:
3 primary part memory means for storing data;
4 independent backup part memory means for storing data;
5 connection means for selectively substituting an operational I/O data line of said backup memory
6 means for a failed I/O data line of said primary memory means;
7 said memory module has a target memory capacity X,
8 said primary part memory means has a memory capacity X minus the capacity of any defective I/O
9 data lines therein; and
10 said independent backup part memory means has available memory capacity at least equal to the
11 capacity of said defective I/O data lines.

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1 ⁶⁶ (Amended) ⁶⁵~~67~~. A memory module in accordance with claim [66] ⁶⁵~~67~~ wherein:
2 said connection means comprises a pattern of solder dot connections.

1 ⁶⁷ (Amended) ⁶⁵~~67~~. A memory module in accordance with claim [66] ⁶⁵~~67~~ wherein:
2 said connection means comprises a pattern of jumper wire connections.

1 ⁶⁸ (Amended) ⁶⁵~~67~~. A memory module in accordance with claim [66] ⁶⁵~~67~~ wherein:
2 said primary part memory means comprise 1MX16 parts; and
3 said backup part memory means comprise 1MX4 parts.

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1 ⁷¹~~74~~. (Once amended) [The method of claim 71 further comprising:] A method for constructing a fully
2 functional memory module which utilizes partially defective independent memory circuit parts
3 comprising:
4 (a) testing and classifying memory parts in a set of defined classifications
5 (b) selecting a primary memory part having a selected classification;
6 (c) selecting a backup memory part having a selected different classification; and-
7 (d) constructing a memory module wherein: any defective data lines of the selected primary memory
8 part are replaced by operational data lines of the backup circuit structure ^{structure};
9 (e) testing said so constructed module as to its operational status to approve use of said module or
10 to identify any operating problem in said module; and
11 (f) reconstructing said module to remove any identified operating problem;
12 (g) testing said module as to its operational status to approve use as reconstructed or to identify
13 any operating problems; and
14 (j) repeating steps (h) and (i) as required until the module is approved for service.